

IN THE SPECIFICATION

Please amend the specification as follows.

The paragraph beginning at page 9, line 18, is amended as follows:

If in operation 220 it is determined that an extraction process is not desired, then processing proceeds to operation 240. In operation 240 it is determined whether a combination process executed by the combination function module 160 ~~condition-check module 175~~ for the arithmetic flags illustrated in FIGs. 1A through 1D is desired. If a combination process is not desired, then processing proceeds to operation 280 where again processing terminates. However, if a combination process executed by the combination function module 160 ~~condition-check module 175~~ is desired for the flags associated with several data items shown in FIGs. 1A through 1D, then processing proceeds to operation 250. In operation 250, the flags for each data item in the SIMD PSR register are extracted based on the field size determined in operation 210. Processing then proceeds to operation 260 where the extracted flags for each data item are combined based upon the function desired. Specific examples of combination functions for an AND operation and an OR operation are further detailed in the discussion of FIG. 4 and FIG. 5, respectively. Thereafter, processing proceeds to operation 270 where the results of the combined flags are stored in the destination register for access by the processor. Processing then terminates in operation 280.

The paragraph beginning at page 10, line 10, is amended as follows:

FIG. 4 is ~~an of~~ a flowchart of an AND function used in an example embodiment of the present invention and may be executed by the combination function module 160 ~~condition-check module 175~~. Processing for this AND operation begins in operation 300 and immediately proceeds to operation 310. In operation 310 it is determined whether the data field size is four bits (one nibble) in length. If the data field size is four bits in length, then processing proceeds to operation 320. In operation 320, bits 31 through 28 of the destination register are set equal to bits 31 through 28 ANDed with bits 27 through 24 ANDed with bits 23 through 20 ANDed with bits 19 through 16 ANDed with bits 15 through 12 ANDed with bits 11 through 8 ANDed with

bits ~~[[the]]~~ 7 through 4 and 3 through 0 of the SIMD PSR register. Thereafter, processing proceeds to operation 330 where the remaining bits 27 through 0 of the destination register are set to zero. Processing then proceeds to operation 395, where processing terminates.

The paragraph beginning at page 11, line 15, is amended as follows:

FIG. 5 is ~~an~~ of a flowchart of an OR function used in an example embodiment of the present invention and may be executed by the combination function module 160 ~~condition-check module 175~~. Processing for this OR operation begins in operation 400 and immediately proceeds to operation 410. In operation 410 it is determined whether the data field size is four bits (one nibble) in length. If the data field size is four bits in length, then processing proceeds to operation 420. In operation 420, bits 31 through 28 of the destination register are set equal to bits 31 through 28 ORed with bits 27 through 24 ORed with bits 23 through 20 ORed with bits 19 through 16 ORed with bits 15 through 12 ORed with bits 11 through 8 ORed with ~~[[the]]~~ bits 7 through 4 ORed with bits 3 through 0 of the SIMD PSR register. Thereafter, processing proceeds to operation 430 where the remaining bits 27 through 0 of the destination register are set to zero. Processing then proceeds to operation 495 where processing terminates.

The paragraph beginning at page 12, line 20, is amended as follows:

FIG. 6 is a flowchart of an EXTRACT function used in an example embodiment of the present invention and may be executed by the combination function module 160 ~~condition-check module 175~~. The extract function begins execution in operation 500 and immediately proceeds to operation 510. In operation 510, it is determined whether the data field illustrated in FIG. 1A for the SIMD word is four bits (one nibble) in length. If the data field is determined to be four bits in length, in operation 510, then processing proceeds operation 520. In operation 520, bits 31 through 28 of the destination register are set equal to one of selected nibbles 7 through 0 of the SIMD PSR register. Thereafter, processing proceeds to operation 570 where processing terminates.